REMARKS

Reconsideration and allowance are requested.

Most of the claims stand rejected under 35 U.S.C. §102 for anticipation based on Godfrey. This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Godfrey fails to satisfy this rigorous standard.

The Examiner maps the external memory 200 of Godfrey to the claimed memory and the recited "system bus" to the internal bus 100 of Godfrey. The Examiner suggests that bus 100 is connected to memory 200 *via* the scan path. This is the case. Figure 2 clearly shows that it is the only the device state registers 104a, 108a, 116a, etc. within the peripheral units 102, 106, a110, 114, etc. that are connected to the scan path—not the internal bus 100. The internal bus 100 is only shown coupled t the non-state registers 104b, 108b, 112b, 116b, etc. The scan path is clearly shown is a separate path from the internal bus 100. A single configuration scan data out pin OUT is coupled to the external memory, and the configuration scan data from each peripheral is "sequentially shifted out of each configuration register into external memory 200 via SCAN_PATH. Likewise, the external memory 200 is coupled to the input pin IN, so that configuration scan data from external memory 200 can be synchronously shifted into each peripheral configuration register via SCAN_PATH." Col. 5, lines 1-6. There is no mention of connecting the bus 100 to the memory via the scan path. Nor can the scan path be the claimed

system bus that transfers multi-bit wide data words meaning that multiple bits are transferred in parallel. The one wire scan path transfers data serially. Hence, Godfrey's system bus 100 is not coupled to the memory 200, and thus, the anticipation rejection is improper.

Furthermore, the system bus 100 in Godfrey does not transfer multi-bit data words between the circuit and the memory 200 in response to memory transfer requests issued upon the bus 100 during normal processing operation as recited in the independent claims. The external memory 200 is only connected to the scan path. Godfrey does not teach using the scan path during normal processing operations. As noted above, the scan path in Godfrey is a serial data path and does not transfer multi-bit data words.

The claimed state saving control by the state saving controller is also not present in Godfrey. In Godfrey, the state saving takes place via the scan path and not via the system bus 100. There is no sequence of memory write requests on the system bus 100 that writes one or more state saving multi-bit data words representing the state data values into the memory 200. Also, Godfrey's data transfer does not take place in the form of multi-bit data words, rather it takes place as a serial data signal.

Lacking multiple features recited in the claims, the anticipation rejection is improper and should be withdrawn. The application is in condition for allowance.

Respectfully submitted,

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